REMARKS/ARGUMENTS

I. Introduction

Claims 1-9 and 11-30 have been canceled to simplify the issues before the Examiner. Claim 10 has been rewritten in independent form. Accordingly, claim 10 is the only pending claim.

The present amendment rewrites claim 10 in independent form and cancels the other pending claims. The amendment does not raise new issues and should be entered. **Applicants request that the amendment be entered even if the Examiner is not ready to allow the case so that the Application will be in better condition for purposes of Appeal should the Examiner intend to maintain the finality of the rejection.**

Early in June, Applicants undersigned representative called the Examiner and requested a telephone interview and, alternatively, at a minimum, clarification of the rejection of claim 10 since, in Applicants' opinion, the rejection failed to clearly identify what the Examiner contended in the prior art corresponded to the multiple sets of video context information recited in claim 10.

During the request for an interview Applicants' representative noted Applicants willingness to cancel all the claims but for claim 10 and also noted that the Examiner's response to the previous office action failed to address the elements added to claim 10 in the previous response. Furthermore, the Office Action did not Address

Applicants' arguments with regard to claim 10 other than by citing a broad section of the Purcell patent which does not seem to disclose or describe storing the recited context information.

The Examiner refused to grant Applicants' interview request noting that the Office Action was final and Applicants were not entitled to an interview as a matter of right. The Examiner also declined to clarify the rejection of claim 10 recommending instead that Applicants file a response to the final Office Action and await an advisory or other action in reply to the response.

Given that the Examiner declined Applicants' request for an interview and Applicants request to provide clarification of the rejection of claim 10 so that Applicants could hopefully provide a detailed response, Applicants have had to proceed based on the limited information available in the Final Office Action with regard to claim 10.

This response generally repeats the arguments with regard to claim 10 made in the previous response since the arguments remain valid and the Examiner has not identified in the applied reference the elements present in claim 10.

In view of the following remarks it should be appreciated that Claim 10 is patentable over the applied reference.

II. The Features of Claim 10 are Not Obvious or Anticipated

Claim 10 is patentable because it recites, in pertinent part:

> storing in the decoder circuit **multiple sets of context information for different video streams at the same time**, each set of stored context information corresponding to a different one of a plurality of encoded video data streams processed by the decoder circuit each set of context information including vertical size, horizontal size and frame rate information. (bold and underlining added for emphasis)

Applicants previously argued, and currently argue, with regard to claim 10:

> The storing of multiple sets of context information of the type described allows the decoder circuit to be used to decode multiple bitstreams, e.g., in order to support picture-in-picture capabilities without the need for the information to be transmitted to the circuit each time a different one of the bitstreams is to be decoded. (See Application page 19) **This novel storage of multiple sets of context information is not disclosed in any of the applied references.**

As noted above, the Examiner failed to specifically respond to Applicant's arguments with regard to claim 10 and merely cited a general portion of the Purcell patent which describes decoder 202. In particular, in rejecting claim 10, the Examiner cites col. 17, lines 44 through col. 18, line 16 of the Purcell patent. This portion of the reference states:

Decoder Coprocessor 202

Referring back to FIG. 3, the decoder 202 comprises the code memory 305, decode memory 306, decode logic 307, zigzag logic unit 308, zigzag memory 309, quantizer unit 311 and quantizer memory 310. The zig.sub.-- zag logic unit 308, zig.sub.-- zag memory 309, quantizer unit 311 and quantizer memory 310 can be implemented by the structures disclosed in either of the following applications: a) U.S. patent application entitled "System for Compression and Decompression of Video Data using Discrete Cosine Transform and Coding Techniques," by A. Balkanski et al., now U.S. Pat. No. 5,196,946 issued on Mar. 23, 1993, Ser. No. 07/494,242, filed Mar. 14, 1990, and assigned to C-Cube Microsystems, which is also the assignee of the present application; and b) U.S. patent application entitled "System for Compression and Decompression of Video Data Using Discrete Cosine Transform and Coding Techniques," by A. Balkanski et al., Ser. No. 07/572,198, filed Aug. 23, 1990 now U.S. Pat. No. 5,253,078 issued on Oct. 12, 1993, assigned to C-Cube Microsystems, which is also the assignee of the present application. The above Applications a) and b) are hereby incorporated by reference in its entirety.

The code memory 305 and the Decoder memory 306 implements FIFO memory which overflows into the external DRAM. As coded data arrive on the code bus 207, they are pushed on the FIFO. The coded data in code memory 305 are transferred 64 bytes at a time, assisted by processor 201 using an interrupt mechanism. The coded data are provided to decoder logic unit 307 for decoding. Decoder logic unit 307 generates a "pop" request when it is ready to receive the next coded datum. In one mode of the present embodiment, the code memory 305 and the decoder memory 306 are connected together. In this mode, no part of the FIFO memory reside in the external DRAM.

The low level coded data stream consists of variable length codes, having the syntax defined in the MPEG standard provided in Appendix A. The syntax of the coded data is of the type which parsing can be performed by a finite state machine. (In fact the syntax is defined in section 3 of Appendix A as a finite state machine in pseudo-code form).

Applicants have reviewed the general portion of the Purcell reference cited by the Examiner and quoted above.

The cited portion of the Purcell patent does not disclose or describe multiple sets of context information for different video streams let alone that such information should be stored in the decoder circuit at the same time. Accordingly, **the rejection of claim 10 should be withdrawn.**

III. Request for Clarification

If the Examiner persists in the rejection of claim 10, it is respectfully requested that the Examiner:

1) specifically identify what the Examiner contends in the reference corresponds to:

a set of **video context information** including **vertical size, horizontal size and frame rate information.** (To avoid a repeated rejection based on the Examiner's earlier position Applicants remind the Examiner that the different encoded data streams cited by the Examiner to reject claims 10, 11, 12 and 13 in the Purcell patent in the first office action were not different video data streams but rather streams corresponding to different types of data, e.g., audio, video, etc.)

2) where in the Purcell patent is it described that **multiple** sets of such information **are stored at the same time in a decoder circuit,** e.g., circuit 202 (if the Examiner contends that this is the circuit which corresponds to the decoder circuit of claim 1).

3) **If the Examiner relies on some inherency argument,** e.g., taking the position that the decoder circuit 202 of Purcell MUST store the claimed set of context information, please explain the basis for this inherency arguement, e.g., **what element of decoder circuit 202 must use vertical size information, what**

element of decoder circuit 202 must use horizontal size information and what element of decoder circuit 202 must use frame rate information? Note that the decoding functionally in the claim is distributed and the Examiner contends that distribution of decoder functionality is taught in the Purcell patent. Accordingly, Applicants submit that unless all of the context information elements need to be stored for some processing performed by the specific decoder circuit 202 an inherency argument can not be supported.

4) **If the Examiner identifies a set of context information having the claimed elements but can not identify a second set (as required for there to be multiple sets)** of the context information corresponding to a different video stream being stored in the decoder circuit at the same time, but still contends that this is obvious or inherent, **Applicants respectfully request that the Examiner provide the basis for any new or repeated obviousness or inherency based rejection in an Affidavit or cite a specific portion of a reference in support of the Examiner's position.** Applicants see no indication that the Purcell decoder circuit 202 performs decoding on multiple different video streams, e.g., in parallel. It seems to process a single video stream and therefore there is no reason to store context information corresponding to multiple different video streams at the same time. Applicants note that there is nothing in the background of the present application that discuss storing multiple sets of context information corresponding to different video streams at the same time and therefore the background of the present application

can not make up for the deficiency of the applied reference.

IV. Claim 10 is Patentable

In view of the above discussion, it should be appreciated that claim 10 is patentable because it recites:

> A method of decoding encoded image data comprising the steps of:
>
> **operating a decoder circuit implemented in hardware to perform at least one non-memory intensive image decoding operation to generate, from the encoded image data, a first set of processed image data,** the at least one non-memory intensive image decoding operation being a variable length decoding operation;
>
> **supplying the first set of processed image data** generated by the decoder circuit **to a programmable processor**; and
>
> **operating the programmable processor to perform at least one additional image decoding operation using the first set of processed image data;**
>
> wherein the step of operating the decoder circuit, includes the step of performing at least two additional operations from the group of operations consisting of an inverse scan conversion operation, an inverse quantization operation, an inverse discrete cosine transform operation, and a data reduction operation, the two additional operations being different from said at least one non-memory intensive operation;
>
> **wherein the programmable processor is coupled to a graphics processor**, the method further comprising the steps of:
>
> **operating the graphics processor to perform a motion compensated prediction**

operation using data included in the first set of processed data; and

storing in the decoder circuit multiple sets of context information for different video streams at the same time, *each set of stored context information corresponding to a different one of a plurality of encoded video data streams* processed by the decoder circuit each set of context information including *vertical size, horizontal size and frame rate information*.

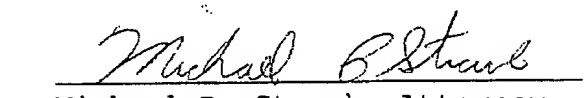
V. Conclusion

In view of the foregoing amendments and remarks, the applicants respectfully submit that pending claim 10 is in condition for allowance. Accordingly, the applicants request that the Examiner pass this application to issue.

Applicants request that the Examiner contact Applicants' undersigned representative by phone if any outstanding issues remain to be resolved to place the application in condition for allowance.

Respectfully submitted,

June 22, 2004



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